
# GLAST Large Area Telescope
## Calorimeter Subsystem

## 7.0 Electrical

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# Electrical Design Overview

- **Electrical Outline**
  - Requirements
  - Electrical Subsystem Architecture
  - Changes since PDR
  - Schedule
  - AFEE Circuit Board, status
  - GCFE ASIC Design, status
  - GCRC ASIC Design, status
  - Preliminary Cal EM Test Results
  - Power, Thermal, Reliability
  - Procurements status
  - ASIC Screening
  - Electrical Documentation status
  - Risks, Issues, Concerns

# Electrical System Requirements (1)

- **Energy Measurement Dynamic Range**
  - Log end electronics shall process energy depositions in the 2 MeV to 100 GeV range
  - The low energy charge amplifier shall process energy depositions in the 2 MeV to 1.6 GeV range
    - The light yield measured by the large PIN photodiode shall be 5000 e-/MeV for energy depositions at the center of the CsI crystal
    - The equivalent noise (RMS) on the low energy slow shaped signal paths shall be less than 2000 e–, for maximum diode capacitance 90 pF
  - The high energy charge amplifier shall process energy depositions in the 100 MeV to 100 GeV range
    - The light yield measured by the small PIN photodiode shall be 800 e-/MeV for energy depositions at the center of the CsI crystal
    - The equivalent noise (RMS) on the high energy slow shaped signal paths shall be less than 2000 e– for maximum diode capacitance 25 pF

# Electrical System Requirements (2)

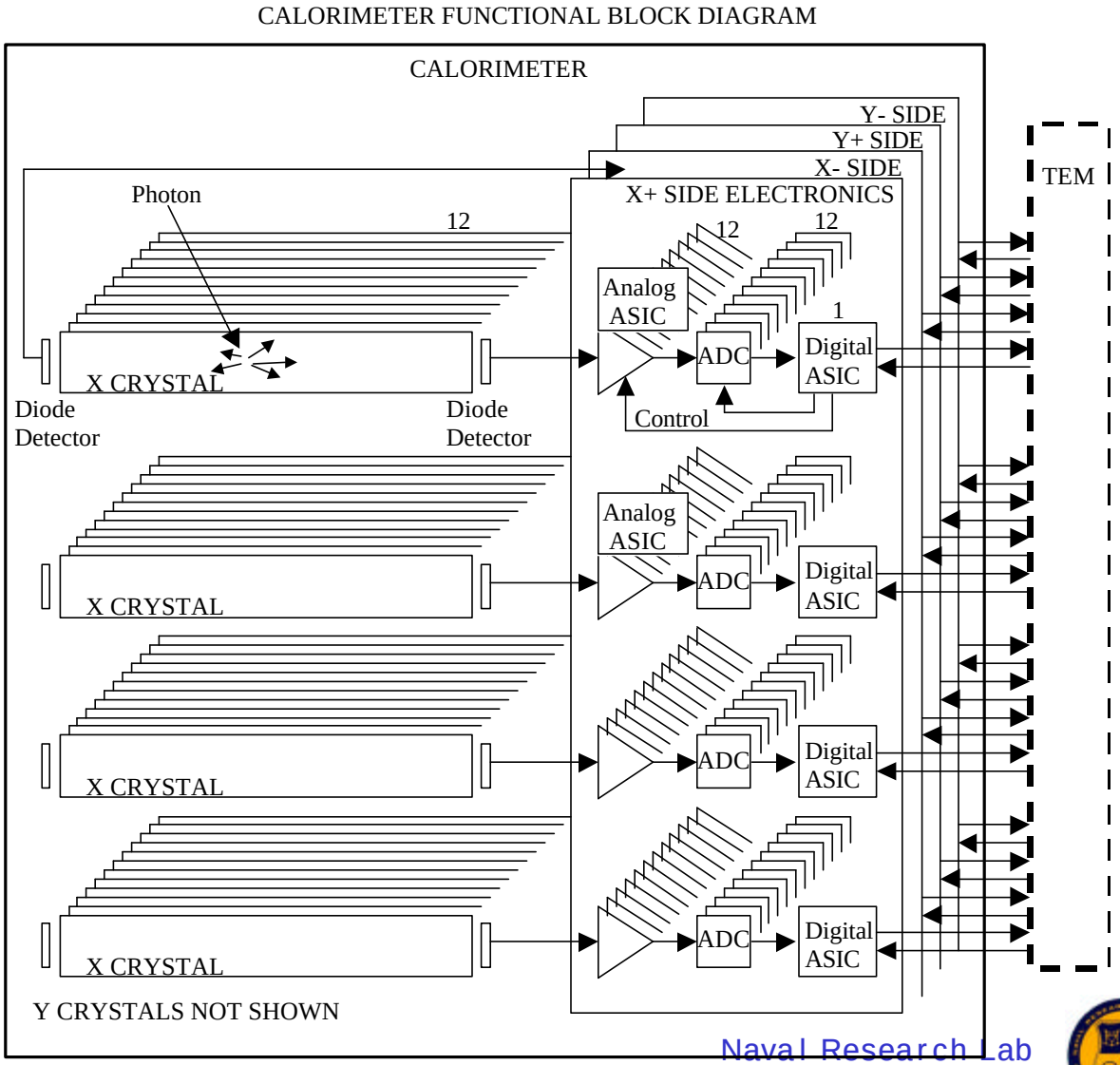
- **Dead Time and Overload**
  - The dead time associated with the capture and measurement of the energy depositions shall be less than 100 μsec. The goal is less than 20 μsec
  - The calorimeter electronics shall be capable of recovery from a x1000 overload within 100 μsec. Recovery is defined as below the measurement readout (zero suppression) threshold
- **Cal Triggers**
  - The calorimeter shall provide a prompt (within 2 μs of an event) low-energy trigger signal to the LAT trigger system with a detection efficiency of greater than 90% (TBR) for 1 GeV gamma rays entering the calorimeter from the LAT field of view with a trajectory which traverses at least 6 Radiation Lengths of CsI
  - The calorimeter shall provide a prompt (within 2 μs of an event) high-energy trigger signal with a detection efficiency of greater than 90% for 20 GeV gamma rays entering the calorimeter from the LAT field of view that deposit at least 10 GeV in the CsI of the calorimeter

# Electrical System Requirements (3)

- **Power**
  - The conditioned power consumption of each calorimeter module shall not exceed 5.6875 W (modified to 4.0 W, pending CCB action)
- **Circuit geometry**
  - Each calorimeter module shall include analog and digital readout electronics (AFEE) on the four vertical faces at the ends of the CsI crystal array
- **Temperature**
  - The performance of the qualification electronics shall be tested over the qualification temperature range of –30 to 50 degrees C
  - The performance specifications of flight units shall be achieved over the operational temperature range of –10 to +25 degrees C
- **Radiation Susceptibility**
  - The electronics shall be insensitive to Single Event Upset for LETs < 37 MeV/(mg/cm$^2$)
  - The electronics shall meet its performance specifications after a total radiation dose of 10 krad (includes margins)
  - Calorimeter electronics latchup requirement: LET > 60 MeV/(mg/cm$^2$)

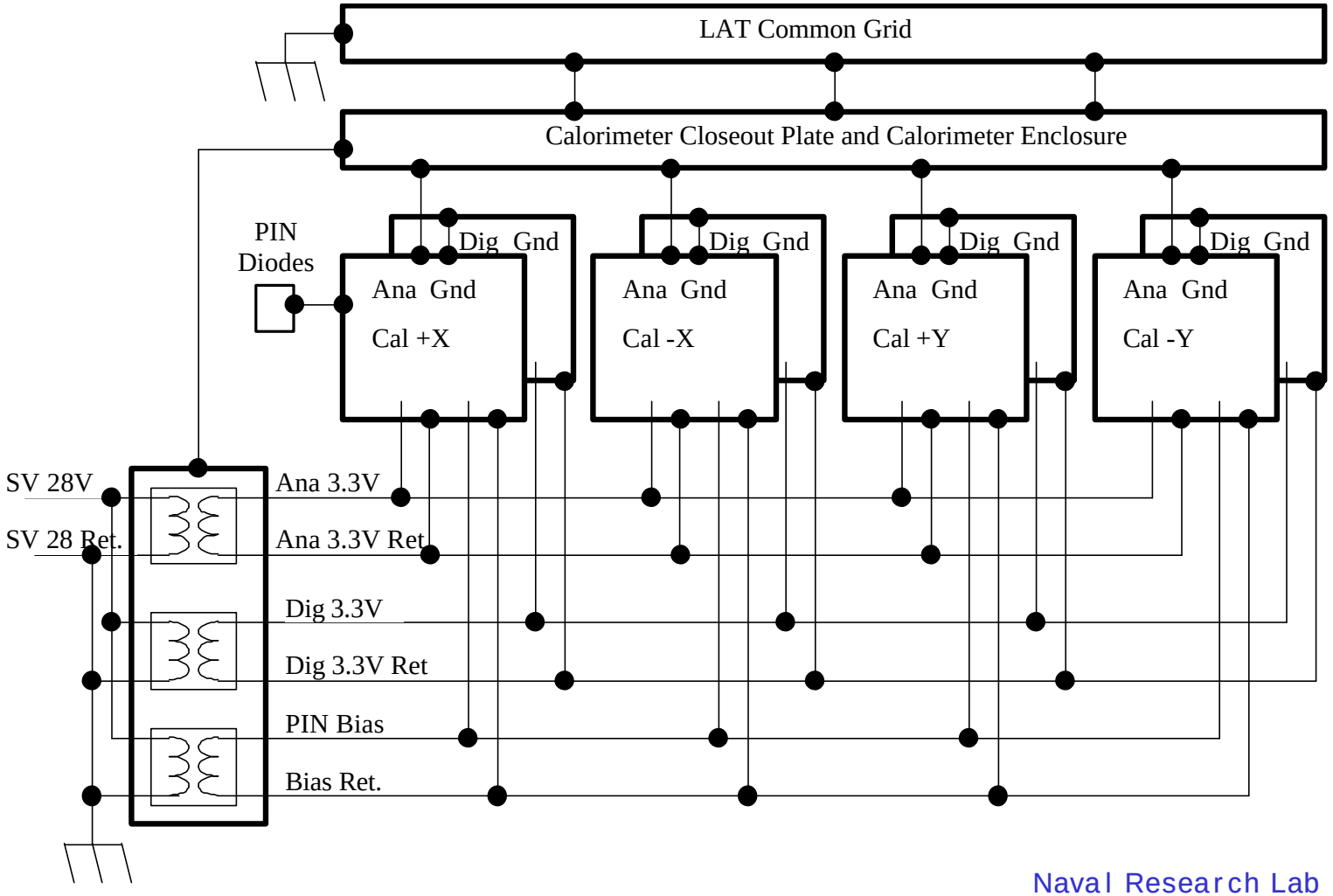
# Electrical Subsystem Architecture

- 1 Cal electronics board (AFEE) per calorimeter side
- Each Cal circuit board communicates to Tower Electronics Module (TEM) mounted below calorimeter
- The TEM correlates crystal end readouts, zero-suppresses the AFEE data and formats the event message for the T&DF
- Redundant system, CAL can operate with loss of 1 X and 1 Y side



# Architecture, Grounding Diagram

- **Calorimeter Circuit boards are grounded to the Cal structure, for low noise PIN diode signal**



# Electrical Changes Since PDR

- AFEE Board Redesigned by SLAC
  - Main change: PIN diode interconnect changed from Kapton Flex cable to AWG 28 twisted pair wiring
- Removed fuses from AFEE board.
  - Cannot get small amperage ( < 0.5 Amp) slow blow fuses
  - Small amperage FM08 fast fuses tend to blow with inrush current
  - FM08 reliability for space flagged as risky
  - TEM board will have 2 fuses (analog and digital power) for each AFEE board
- Rigid-flex AFEE board construction changed to rigid
  - Rigid construction less risk, but more expensive for extra connectors and cables required

# Electrical Schedule (1)

- **Items to complete prior to flight AFEE board assembly**
  - **Verify that GCRC and GCFE ASIC designs are stable and flight ready**
    - **GCRCv5 returning from fabrication is expected to be a flight ready design**
    - **Need to verify LVDS communication is reliable with new chips**
  - **Radiation testing of all flight electronic components**
    - **Write radiation test report, design circuits for single event upset and latchup testing, perform tests**
  - **Write ASIC test documents and fully develop test systems for screening GCRC and GCFE ASICs**
  - **Test and screen all flight GCRC and GCFE ASICs**
  - **Contract to outside vendor to perform burn-in of electrical components**
  - **Setup contract with outside vendor for machine assembly of flight AFEE boards**

# Electrical Schedule (2)

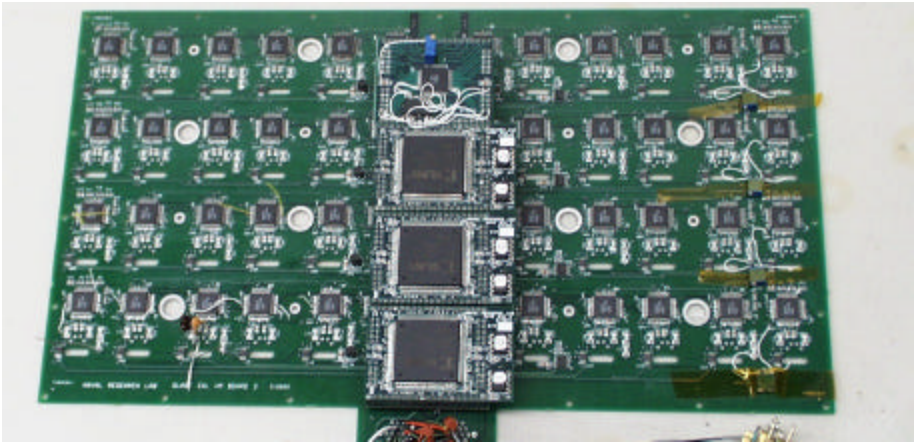
- **Items to complete prior to Assembled Cal Module Delivery to SLAC**
  - **Develop AFEE burn in test prior to AFEE card attachment to calorimeter mechanical structure**
  - **Perform environmental testing of flight units**

# AFEE Board Requirements

- Provide for interconnect between PIN diodes and readout electronics
- House components which will communicate with TEM electronics for electronics configuration setup and CsI crystal event data readout
- Designed to use Mil-Spec NASA approved components when possible. Other commercial components need qualification

# AFEE Board Evolution (1)

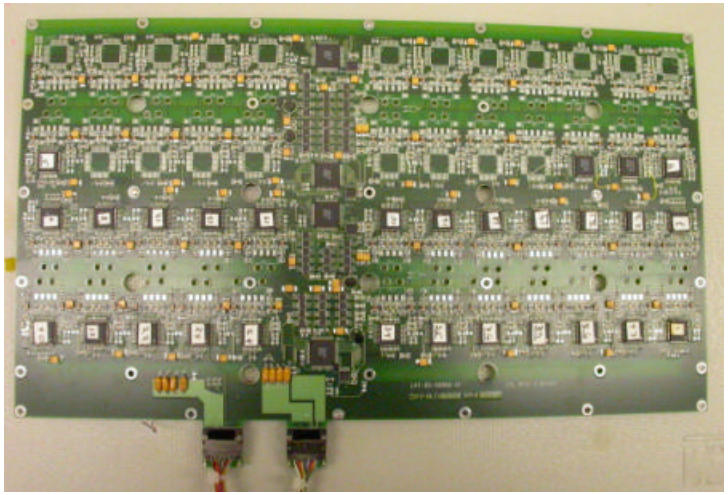
- **VM1 Board, NRL, Oct 01, single row electronics**
  - Some LVDS communications corrupted by CMOS level digital signals through SMT Footprint Extender. Footprint extender used for Xilinx GCRC simulator
  - Jumpered sensitive signals around connector path to get circuits functioning
  - Used for testing VHDL Code in FPGA for GCRCv1, v2 and v3 submissions
- **VM2 Board, NRL, Feb 02, whole 4 row electronics**
  - Used for testing VHDL code in FPGAs for GCRCv4 and GCRCv5
  - Designed custom socket connections between board and FPGA modules to keep LVDS signals away from CMOS level signals. FPGA module could be replaced by soldered ASIC or socketed ASIC
  - Boards used extensively for system software development
  - LVDS Communications at 20 MHz was marginally not working between early versions of GCRC and GCFE chips. At room temp and above some GCFE registers did not read back correctly
  - VM2 Board still used for testing GCRCv4 ASICs used to populate the engineering model boards



Cal VM2 Board Shown with 3 FPGA modules (center) and 1 soldered ASIC module (top) with external buffer wired.

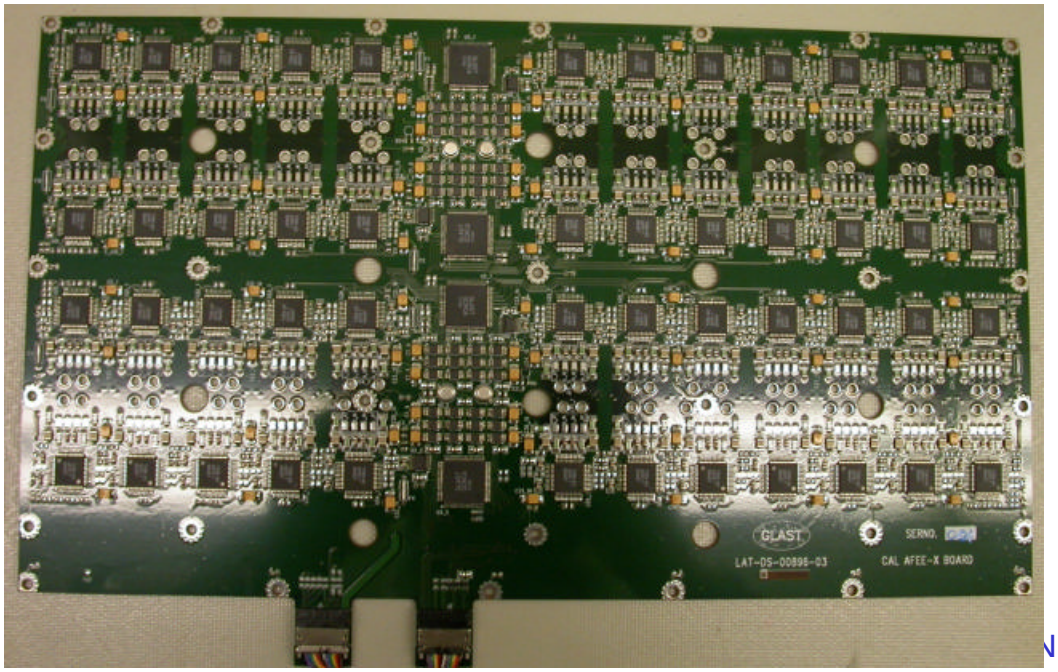
# AFEE Board Evolution (2)

- **AFEE-X Pre-EM Board, SLAC, Aug 02, Redesigned board**
  - SLAC redesigned Cal AFEE board to improve LVDS communications and to make event readout signals quieter as well
    - Capacitance of differential traces to ground thought by SLAC to be problem of unreliable LVDS communication at 20 MHz with existing circuits. New board routing lowered capacitance to ground of LVDS routing traces
  - Board Topology Modified:
    - PIN diode connection to AFEE board changed from shortest path connection with printed Kapton flex cable to discrete twisted pair wiring which allows various horizontal re-directions between diodes and front-end electronics
    - All electronics components put on topside. This enabled space for horizontal routing of diode connection wires between AFEE board and closeout plate
    - Digital electronics grouped approximately in center of board, analog electronics placed elsewhere
  - Individual component current limiting resistors eliminated
  - Board testing with recent versions of GCRC and GCFE chips having more LVDS current drive, communications improved to marginally working at 20 MHz



# AFEE Board Evolution (3)

- **AFEE-X and AFEE-Y EM Board, Dec 02, SLAC**
  - **Design slightly modified from Pre-EM design**
  - **Nicely hand-routed board layout**
  - **Four EM boards for calorimeter have been assembled by hand and are currently being mounted to the EM Calorimeter**
  - **LVDS communications marginally working at room temp and 20 MHz rate using GCFEv7 and GCRCv4 ASICs**
    - **Plan to perform qualification of EM boards at 12 MHz system rate**



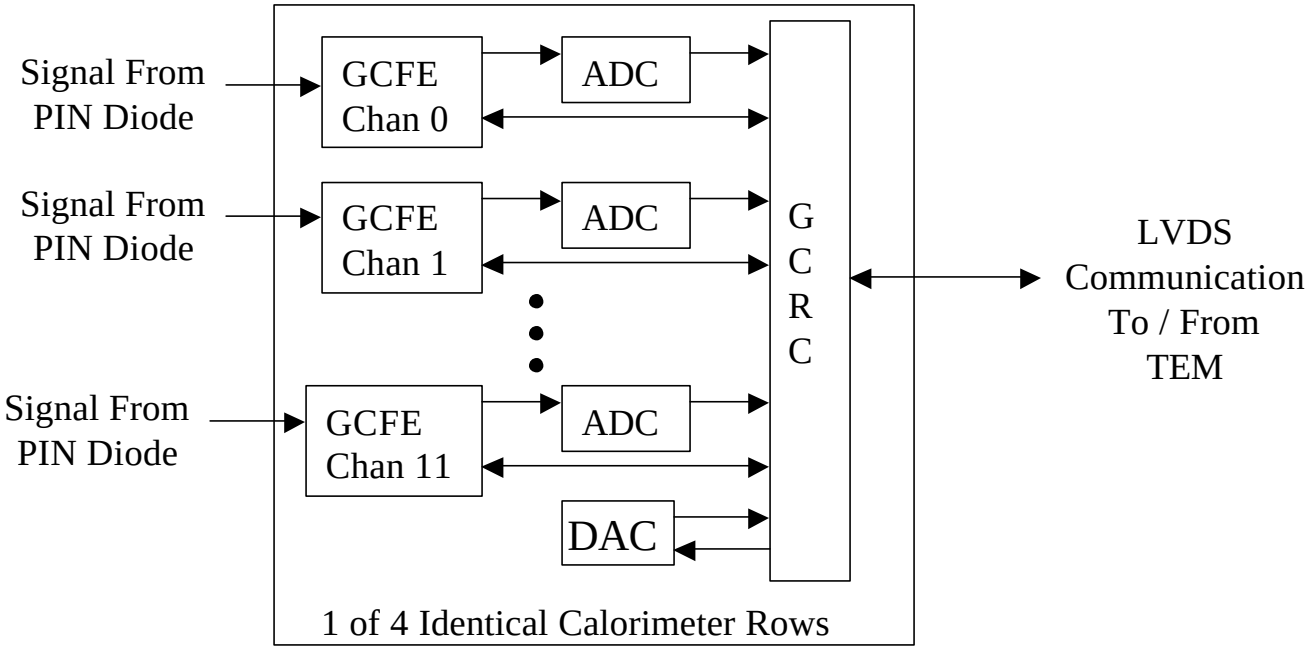

Fully Populated Cal EM AFFE-X Board

# AFEE Design Drivers

- Reliable LVDS communications at 20 MHz between TEM and GCRC ASICS, and between GCRC ASICS and GCFE ASICs
- Low noise self triggering of calorimeter
- Low noise event readout of CsI crystals

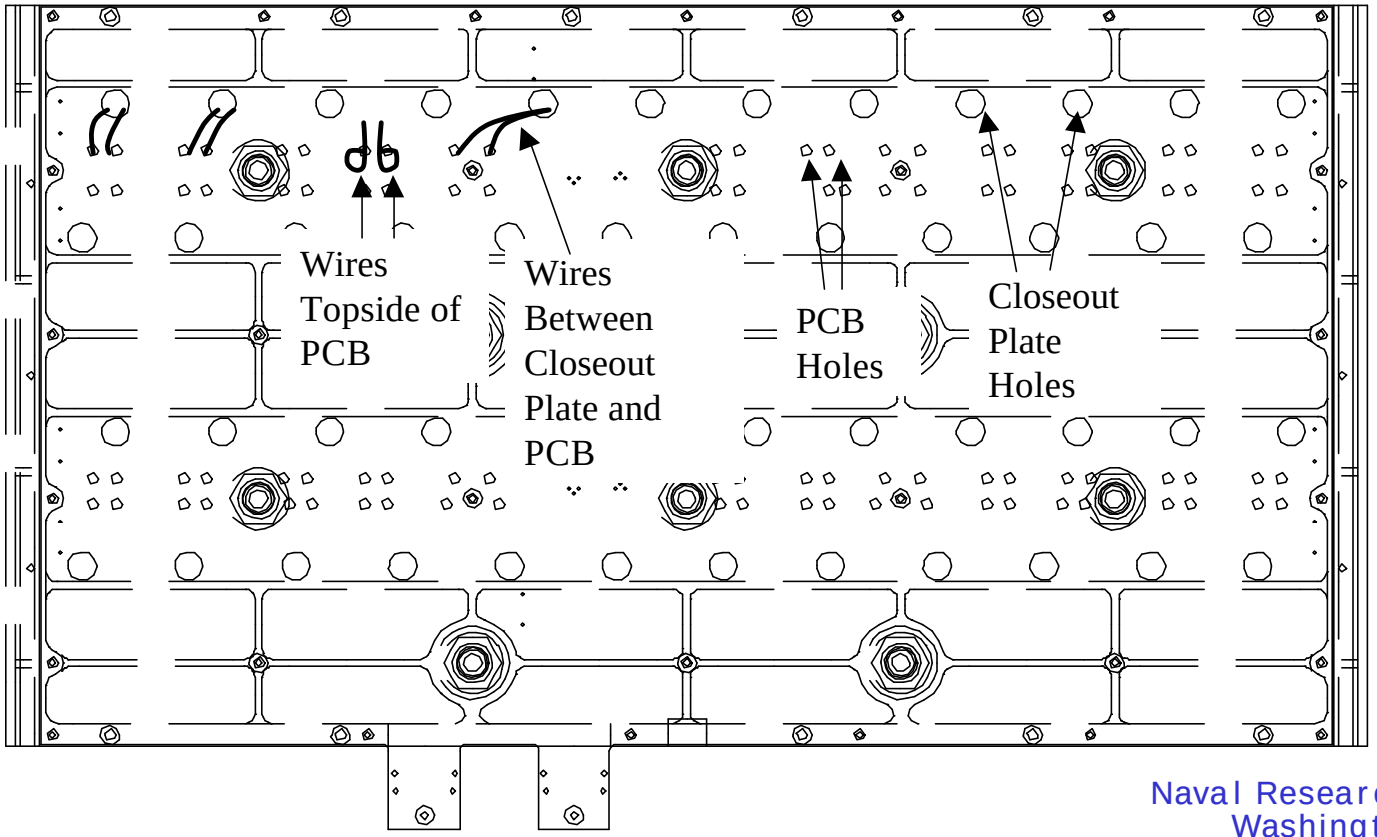
# AFEE Design Details

- **Cal AFEE sideboard design, electronics grouped by rows**
  - **1 analog ASIC (GCFE) and commercial ADC per log end**
  - **1 Digital ASIC per row (GCRC), communicates between GCFE - ADC pair (12 pairs per row) and external TEM**
  - **Partitioned design – communication failure of 1 GCRC only removes 1 row, short circuit failure removes 1 side board. Would still meet mission requirements**



# PIN Diode Connection to AFEE Board

- **Plan View of EM AFEE Board PIN Diode Wiring Holes superimposed over Cal closeout plate. Few diode wire paths sketched in, representing twisted pairs**
  - **Wires staked at diode end and PCB end**
  - **Flight closeout plate to have insulating coating beneath wire runs**
  - **One rework length of wiring (5 mm) added to wire length, contained in loop on PCB**
- **Wire connection to SMT pads is labor intensive. Looking for alternatives for flight.**



# AFEE Parts

- **All Flight Components are Determined**
- **Previously changed from all Cristek connectors to combination of Microdot/Nanonics connectors for Nano 37 contact connector and Airborn for Micro 69 contact connector**
  - **Had two separate shipments with problems from Cristek. In addition to being delivered incorrect product, customer support was very poor. We decided that this company was a flight procurement risk**
  - **Nanonics was previously NASA approved prior to manufacturing facility moved to Microdot. Working on qualification documents following move**
- **Bias resistance values controlling GCFE and GCRC LVDS drive and receive currents, along with LVDS termination resistance values may change following implementation of GCFEv9 and GCRCv5 which are coming back from wafer fabrication**

# AFEE Design Analysis, Charge Collection Efficiency

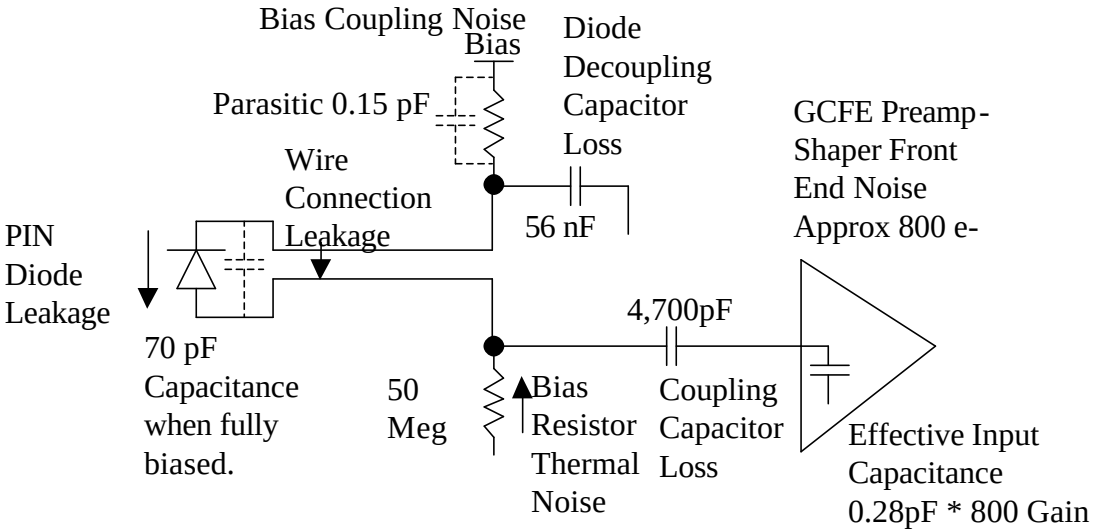
- **Effect of PIN Diode coupling capacitor value on charge collection efficiency. Very low loss with flight cap value**
  - Flight design is to use 4,700 pF 100V cap in 0805 footprint
  - Using Am-241 Source with EM PIN diode, measure the loss of signal vs. coupling capacitor value. Analysis from 10/30/02 memo. Measurements from 3/20/02 memo

| Modeled Coupling Cap from PIN diode to GCFE | LE Worst Case Calculated Peak Loss (0.28 pF preamp feedback, preamp G=800, 70 pF detector ) | HE Worst Case Calculated Peak Loss (1.08 pF preamp feedback, preamp G=800, 10 pF detector ) |
|---|---|---|
| 10,000 pF | 2.3 % | 0.5 % |
| 4,700 pF Flight Value | 2.8 % | 1.2 % |
| 1,000 pF | 5.3 % | 5.4 % |

| Actual Coupling Cap from PIN diode to GCFE | Measured GCFEv4 LE Signal Peak Loss from Maximum | Measured GCFEv4 LE Signal/Noise Loss from Maximum |
|---|---|---|
| 10,000 pF | 0 % | 0 % |
| 1,000 pF | 4.6 % | 3.19 % |
| 220 pF | 15 % | 6.2 % |

# AFEE Design Analysis, Added Front-end Noise

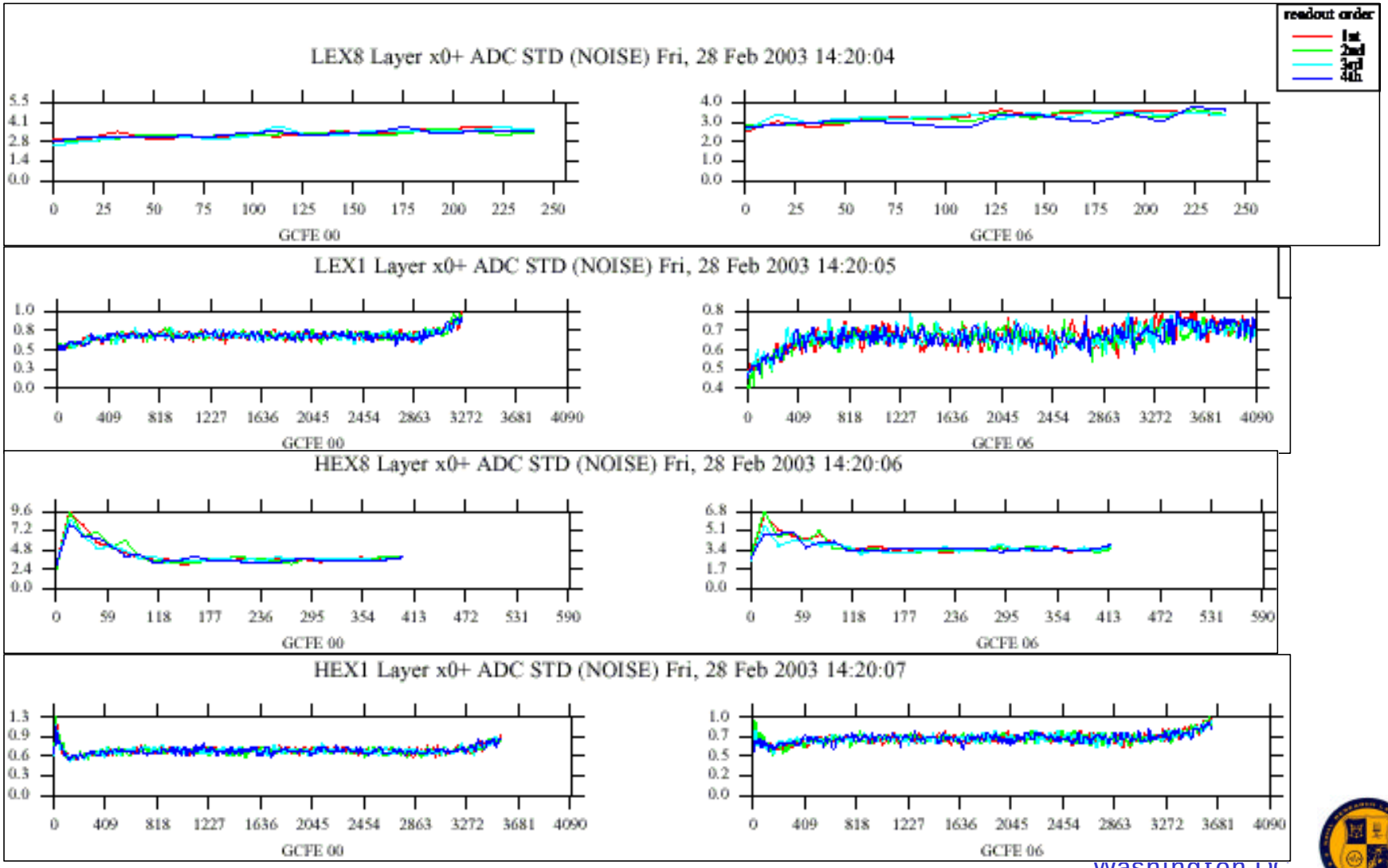
- **Analysis was performed to verify AFEE design added only minimal noise to front-end electronics.** From modified 6/10/02 memo
  - **External noise added in quadrature is 257 electrons, compared to GCFE input referred noise of approx 800 e-. Added in quadrature GCFE output noise is 840 electrons**




| Item | Bias 0.1 mV RMS noise, capacitively coupled in. | Diode Decoupling Capacitor Signal Loss | Pin Diode Leakage Shot Noise, 1 nA | PIN Diode Wire Connection Leakage, 0.1 nA | Bias Resistor Thermal Noise | Coupling Capacitor Signal Loss |
|---|---|---|---|---|---|---|
| Noise Contribution Electrons | 0.11 e- | 0 Loss | 176 e- | 56 e- | 179 e- | 2.8 % |

# AFEE Test Results

- **Sample of AFEE-X SN 001 Noise Test Results. Noise is generally good**



# AFEE Design Summary

- **EM AFEE board design works well all functions except for calibration crosstalk between front-end GCFE chips**
- **List of potential modifications to Cal EM AFEE board for flight:**
  - Tantalum capacitor footprint changed to CWR11 tantalum footprint
  - Length of PCB connector tab shortened by 1.0 mm
  - PIN diode wiring through holes grounded or not plated
  - PIN diode wire through holes horizontally offset from corresponding solder pads
  - PIN diode wire through holes moved away from large 8 mm diameter holes. Hex nut beneath the hole perimeter
  - Capacitance added on GCFE Calib_V lines, for reducing calibration crosstalk
  - Testpoints for important items
    - Each DAC output voltage
    - Each GCFE analog output
    - Board analog supply voltage with corresponding ground test point
    - Board digital supply voltage with corresponding ground test point
    - Each 2.5 volt reference
  - Modification of PIN diode wire connections

# GCFE ASIC Requirements

- **Key GCFE ASIC Requirements. From GCFE Requirements Spec, LAT-SS-00089-D2, Jan 01**
  - **Total Energy Dynamic Range 2 MeV to 100 GeV**

| GCFE Range | LEx8 | LEx1 | LE Fast Shaper | HEx8 | HEx1 | HE Fast Shaper |
|---|---|---|---|---|---|---|
| Energy Range | 2 MeV – 200 MeV | 2 MeV- 1.6 GeV | 2 MeV – 400 MeV | 100 MeV- 12.5 GeV | 100 MeV- 100 GeV | 100 MeV– 100 GeV |

  - **Slow shaper output noise less than 2000 electrons RMS when connected to PIN diode**
  - **Fast shaper output noise less than 3000 electrons RMS when connected to PIN diode**
  - **Slow Shaper peaking time 3.5 +/- 0.5 usec.**
    - **Chip- Chip variation < 0.4 usec**
  - **Fast Shaper peaking time 0.5 usec +/- 0.2 usec**
  - **Integral non-linearity < +/- 0.5% of full scale, over 99% of energy range**
  - **Insensitive to Latchup and total dose effects**

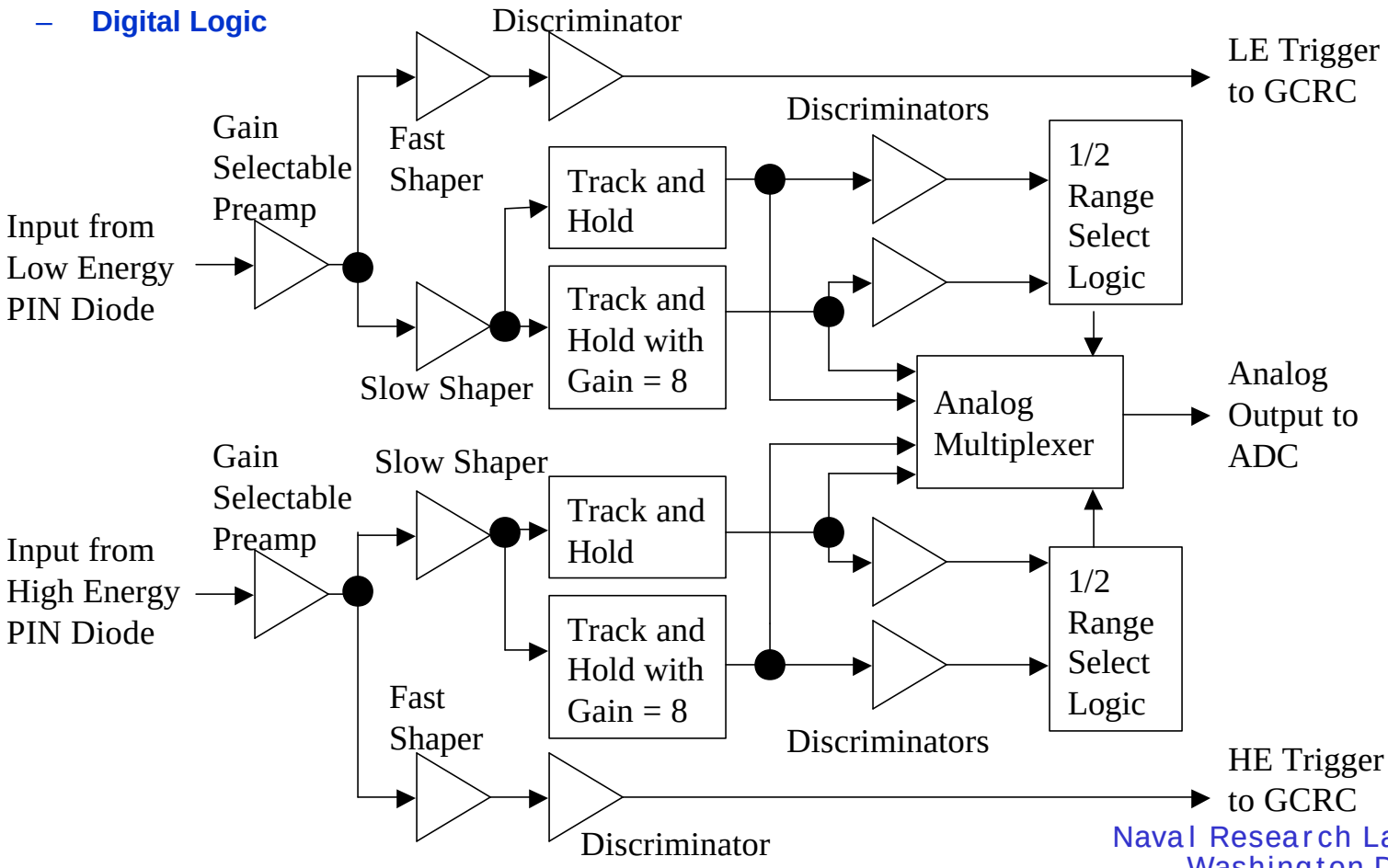
# GCFE Evolution

- GCFEv1 submitted March 01. Not Sent to NRL
- GCFEv2 submitted April 01
- GCFEv3 submitted Aug 01
- GCFEv4 submitted Oct 0
  - Programmable DACs improved
  - Slow shaper R's and C's put on die
  - Preamp gain increased
  - Improved Shaper op-amp for lower noise
  - LVDS receiver current doubled for faster operation
- GCFEv5 submitted Jan 02
  - Changed chip pinout for addition of input guard rings
  - Digital code modified to recognize broadcast address
  - Non-register flip flops changed to non-SEU hard type
  - Pin added for LVDS driver current control
- GCFEv6 Ver 6c submitted April 02
  - 6c corrected Well- Well spacing problem
- GCFEv7 Large fabrication run
- GCFEv8 Submitted Aug 02
  - Output buffer gain increase to get 2.5V linear output range
  - Add circuit for automatic preamp reset actuation. Modify Autoreset trigger gating circuit to prevent spurious triggers
  - Calibration Inject capacitors modified to be able to test autoranging
  - Increase LEx8 and HEx8 Pedestal
- GCFEv9 Flight Fabrication run, Submitted Dec 02
  - Faster LVDS Receiver
  - Auto Range DAC adjustment
  - Increased output buffer compensation and added series resistance

# GCFE Design Details

- **Analog signal path diagram shows four output ranges from two diode inputs**
- **Not Shown:**
  - **Digital to Analog Converters, quantity 6**
  - **Calibration injection circuit**
  - **Digital Logic**

(Packaged in 44 pin QFP, 10 mm sq)

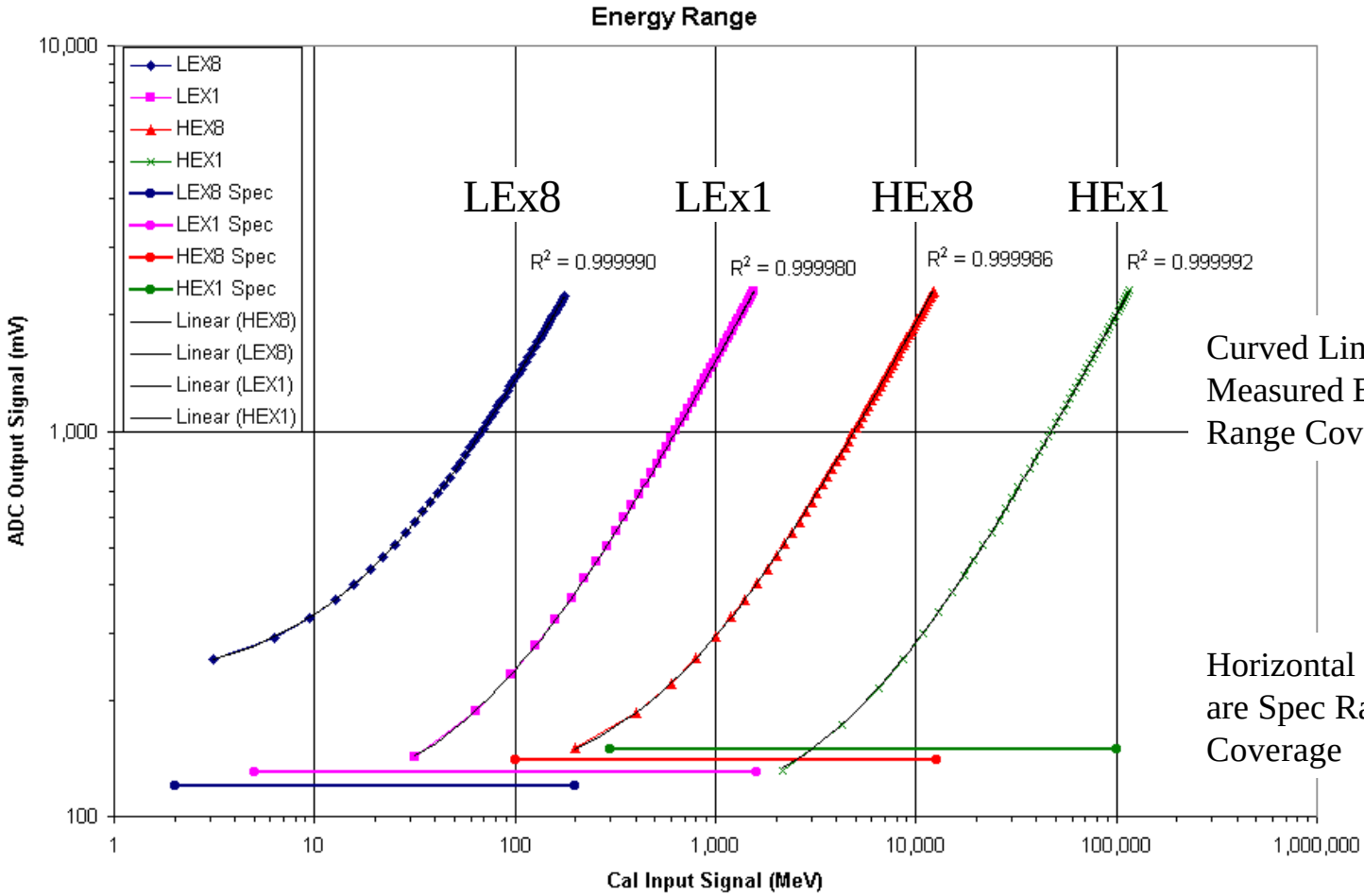


# GCFE v7 Measured Test Results

- Measured Output Noise: Requirement less than 2000 electrons (e-)
  - Use Am-241 Source, measurements from one device.
  - Shaper Output: LEx1 662 e-, Hex1 1045 e-
  - Track & Hold Output: LEx8 760 e-, LEx1 1936 e-, HEx8 1141 e-, Hex1 2633 e-
- Non-Linearity: Requirement less than 0.5% of full scale
  - LEx8 < +/- 0.3%, LEx1 < +/- 0.3%, HEx8 < +/- 0.3%, Hex1 < +/- 0.2%
- Signal Pedestal: No Spec, but > 100 mV for low end linearity purposes
  - LEx8 2.9-188 mV, LEx1 80-131 mV, HEx8 2.9–245 mV, Hex1 78-143 mV
- Energy Range, Upper Limit
  - LEx8 185 MeV, Spec 200 MeV  Lex8 1.56 GeV, Spec 1.6 GeV
  - HEx8 12.2 GeV, Spec 12.8 GeV  HEx1 116 GeV, Spec 100 GeV
- Normalized Gain Ranges
  - LEx1 2.96 to 0.78  Spec 3.04 to 0.79
  - HEx1 10.52 to 0.78  Spec 10.65 to 0.79
- Power Consumption, Spec 8 mW per chip, power budget 11 mW per chip
  - Measured 10.4 mW at 1KHz event readout rate
- Output Range doesn't meet requirement, but acceptable for EM testing
  - Corrected in GCFE v9 – Flight version

# GCFEv7 Energy Range Plot

- **GCFE ASIC Meets Dynamic range specification**
  - Graph from GCFEv7 Test Report LAT-TD-01012-03 10/3/02




Curved Lines are Measured Energy Range Coverage.

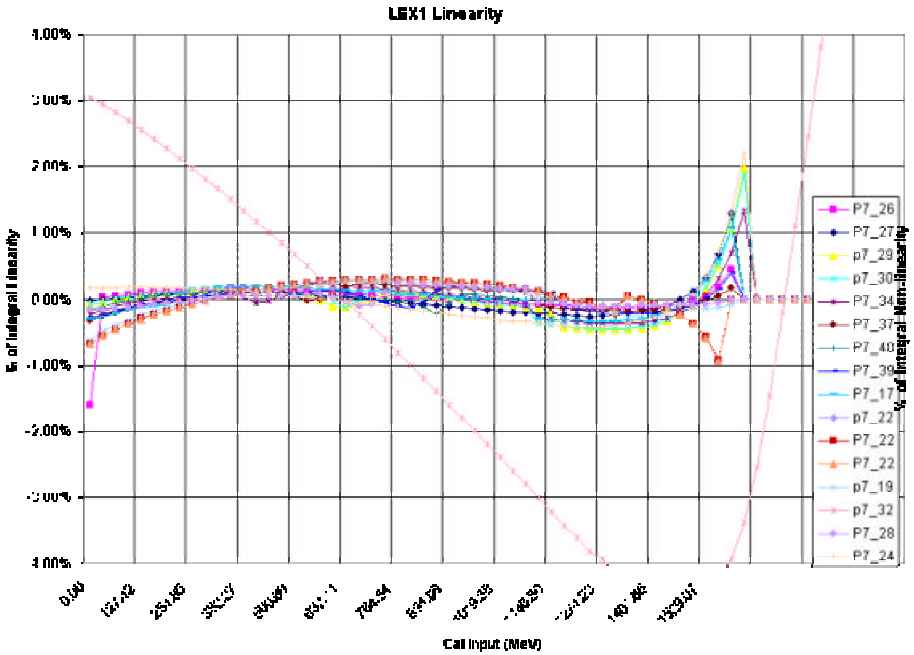
Horizontal Lines are Spec Range Coverage

# GCFEv7 Noise and Linearity Plots

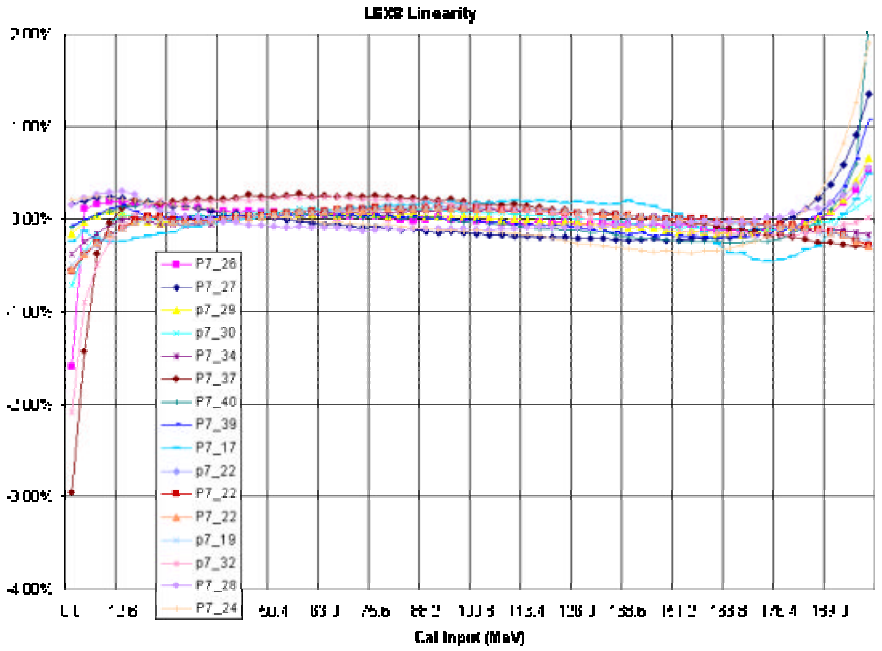
## Linearity over range is good

Graphs from GCFEv7 Test Report LAT-TD-01012-03 10/3/02

LEx1 Linearity




LEx8 Linearity



# GCFE Design Summary

- Noise out of the Track-and-Hold is about 2000 electrons, which meets spec
- Linearity is good, meets spec over most of dynamic range
- Digital control is correct
- Items corrected prior to flight fabrication:
  - LVDS communication problems at 20 MHz.
    - Need to test new GCFEv9 and GCRCv5 coming back from fabrication. Expect problem to be solved with new chip designs
    - System could be run at lower clock frequency
  - Calibration signal coupling between GCFE chips on AFEE Board. Amount of coupling proportional to amount of charge injection and number of chips in the row being calibration strobed
    - Slight annoyance for calibration only
    - Fix could be adding capacitance to DAC voltage lines

# GCRC ASIC Requirements

- Perform electrical interface between TEM and single AFEE board row
- AFEE row communications
  - Write to and Read from 12 GCFE chips
  - Write to and Read from 1 Digital to Analog Converter
- For Event readout
  - Control GCFE chips and ADCs
  - Combine data from ADCs, GCFE log accept bits, GCFE range bits and send to TEM
- Housekeeping
  - Detect communication parity errors
  - Save last command which generated parity error

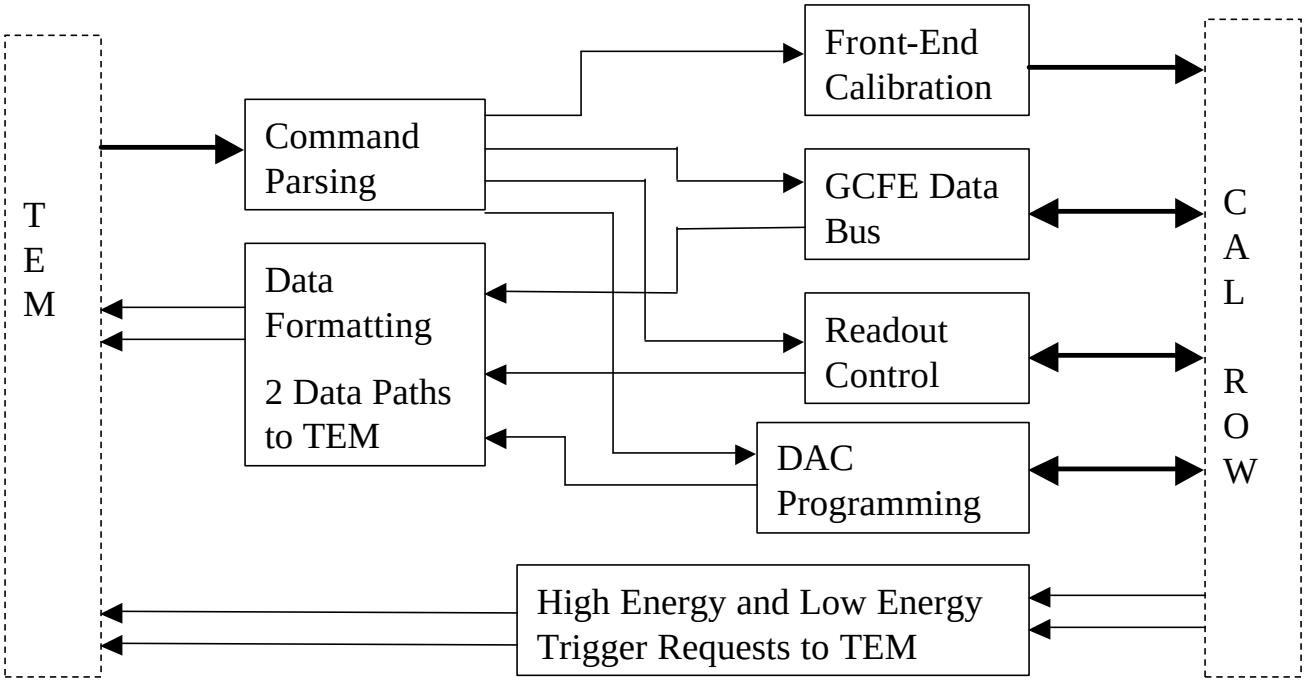
# GCRC Evolution

- GCRCv1 submitted for Fabrication Nov 01
  - Digital outputs not buffered
  - With external buffer driver, chip tested functionally correct
  - Expected input trigger polarity from GCFE chips inverted
- GCRCv2 submitted Jan 02
  - Digital outputs not buffered
  - Re-assign some pins to move 1 digital signal away from LVDS signals
  - Data to GCFE erroneously shifted to left by 1 bit. Compensated for in software
- GCRCv3 not fabbed by Mosis
- GCRCv4 submitted April 02
  - Digital outputs correctly buffered
  - Removed delay from Calib command to Calib strobe
  - Remove trigger request deadtime following digital operations
  - LVDS Driver and LVDS Receiver bias pins added to package
- GCRCv5 submitted Dec 02 Expected flight version
  - Read data back from GCFE at half clock rate, while transmitting data to TEM at full clock rate
  - Updated command addressing to match TEM and ACD
  - Added Reset command implementation
  - Added reset line de-glitching
  - Added readable GCRC VHDL version number hard coded into unused register bits
  - Removed trigger request disable during digital operations

# GCRC Design Details

- **GCRC Digital ASIC, main Features**
  - 1 GCRC per Cal row interfaces 12 GCFEs, 12 ADCs, and 1 DAC to the TEM
  - LVDS communication used for all communication except to ADC and DAC chips
  - Each GCRC has a hard wired address to receive bussed commands from the TEM

(Packaged in 80 pin QFP, 14 mm sq)



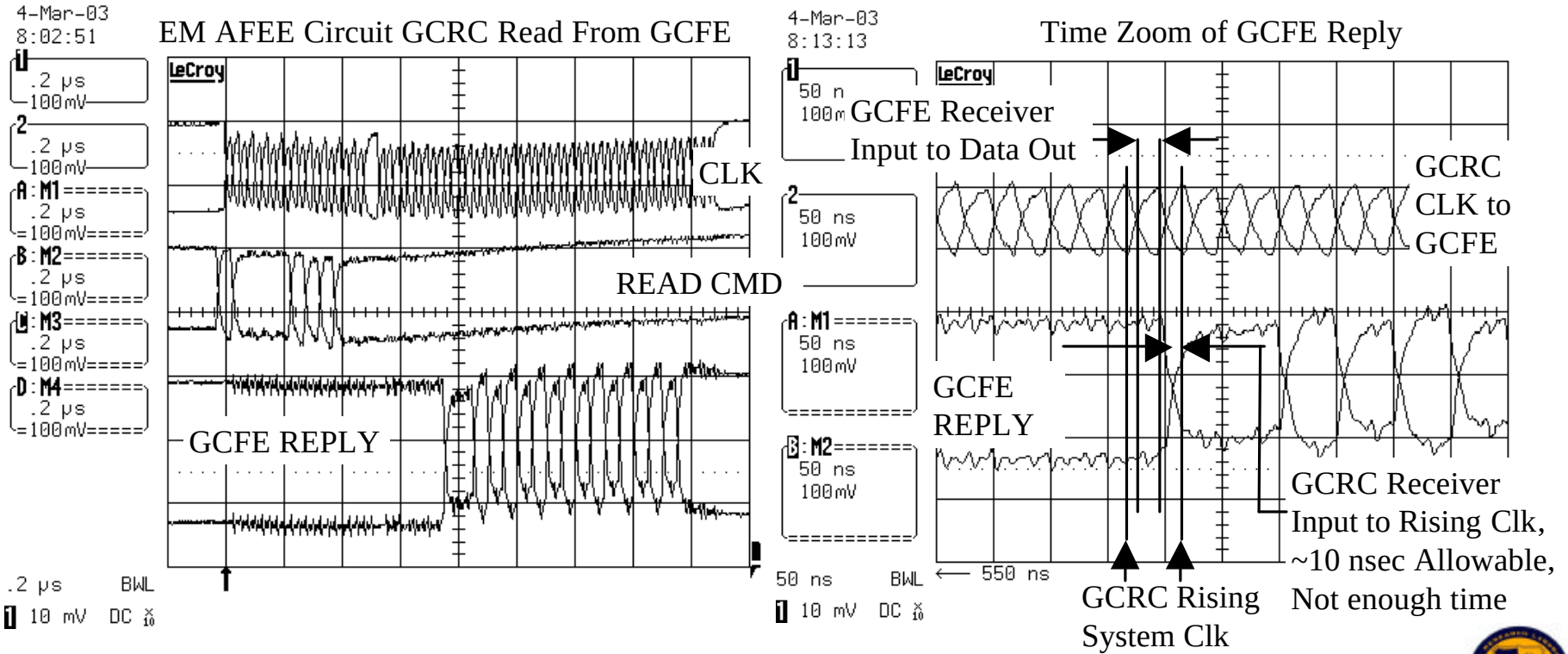
# GCRC Design Analysis, Communication Margins

- GCRC communication rate to external devices with resulting timing margins

| Device | MAX145 ADC | MAX5121 DAC | GCFE | TEM |
|---|---|---|---|---|
| Communication Format | Digital CMOS 3.3V | Digital CMOS 3.3V | LVDS | LVDS |
| Device Specification Maximum Rate | 5 MHz read clock over temp range | 6.7 MHz clock rate over temp range | - | - |
| GCRCv5 Design Communication Rate | 3.3 MHz (1/6 of system clk) read clk rate | 5.0 MHz (1/4 of system clk) write clock rate | 20 MHz Write<br>10 MHz Read (1/2 of system clk) | SLAC Responsibility |
| Timing Margin | 103 nsec | 50 nsec | Writing: 15 nsec timing margin<br>Reading: Desired 10 nsec margin Expect 30 nsec margin with GCRCv5 ASIC | SLAC Responsibility |

# GCRCv4 Test Results, GCFE Communications

- **GCRCv4 to GCFEv7/v8 LVDS Communication on Pre-EM AFEE Board, Failure of Timing Margin**
  - **Setup: Room temp, GCRC termination 100 ohms, GCFE termination 200 ohms**
  - **GCRCv5 will have 100 nsec for data to come back to it instead of the present 50 nsec**
  - **GCFEv9 will have shorter Receiver Input to Data Out delay**



# GCRC Design Summary

- **GCRCv4 Correct Functional Design:**
  - Parity checking, Parity adding, Parity changing
  - Commanding from/to TEM
  - Reading / Writing to GCFE ASIC
  - Controlling and reading of ADCs
  - Programming onboard DAC
  - Merging event readout data from 12 ADCs and 12 GCFEs for transmission to TEM
  - Diagnostics handling
- **Items corrected prior to flight fabrication:**
  - LVDS communication at 20 MHz
    - Need to test new GCRCv5 and GCFEv9 coming back from fabrication. Expect problem to be solved with new chip designs
    - System could be run at lower clock frequency

# Cal EM Test Results

- **First look at Cal EM AFEE board looks good**
  - **AFEE X SN 01**
    - **Only one GCFE chip that does not read back correctly at 20 MHz and room temperature**
    - **All other chips pass extensive register write/read tests**
    - **Linear/noise test looks good**
  - **AFEE X SN 02**
    - **15 GCFE chips not reading back correctly at 20 MHz and room temperature**

# AFEE Power

**Measured Power Estimate per AFEE**

- **(GCFEv9 and GCRCv5 have increased LVDS Receiver bias current)**

| | GCFEv9 1 KHz evt rate | GCRCv5 any evt rate | MAX145 ADC, 1 kHz evt rate | MAX5121 DAC | Reference | Total Power per AFEE board | Total Power per CAL module |
|---|---|---|---|---|---|---|---|
| Analog per AFEE | 230 mW | | | | 27.0 mW | 257 mW | 1028 mW |
| Digital per AFEE | 317 mW | 256 mW | 2.0 mW | 4.5 mW | | 580 mW | 2320 mW |
| | | | | | | | 3348 mW |

**CAL Module Conditioned Power Allocation**

| | Analog 3.3 V | Digital 3.3 V | Bias 100V | Total Allocated Conditioned Power, Analog + Digital | Power Margin, Analog + Digital |
|---|---|---|---|---|---|
| Per AFEE | 300 mW | 700 mW | 1 mW | 1001 mW | 164 mW |
| Per Tower | 1200 mW | 2800 mW | 4 mW | 4004 mW** | 656 mW** |

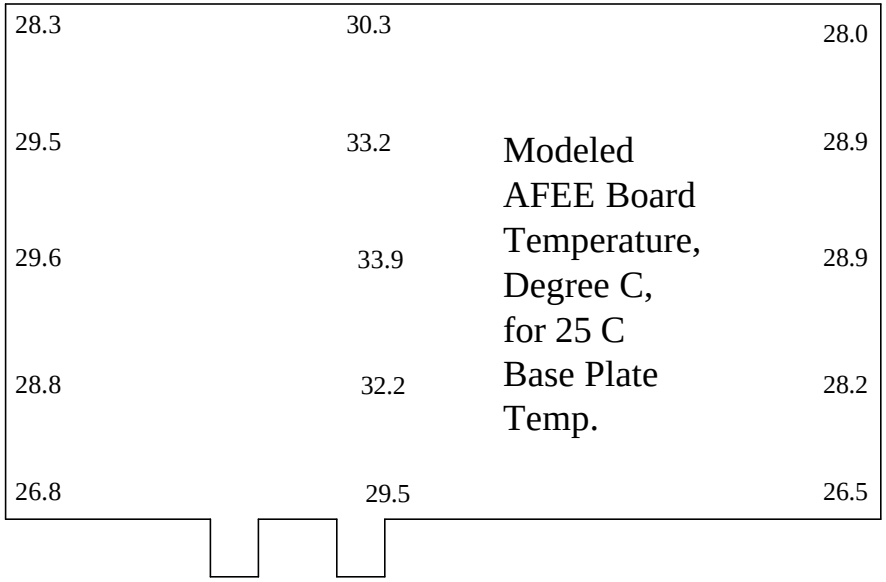
*** Reduced values, pending CCB action***

# AFEE Thermal Analysis

- **AFEE Thermal Analysis Summary.** From LAT-TD-01114-01 Dated 10/02
  Author Peck Sohn, Swales Aerospace
- Table of maximum silicon die temperature for 25 C Base Plate temperature

| Device | GCRC | GCFE | ADC | DAC | Ref. |
|---|---|---|---|---|---|
| Die Junction Temp. Degrees C | 36.2 | 33.5 | 34.5 | 34.3 | 34.8 |

- Analysis result, Calorimeter AFEE electronics do not have any thermal problems




Assumptions

| | Modeled Heat Dissipation | Theta Junction to Board (C/W) |
|---|---|---|
| GCRC | 50 mW | 44.5 |
| GCFE | 10 mW | 105 |
| ADC | 4 mW | 135 |
| DAC | 6 mW | 62.3 |
| Ref. | 15 mW | 57 |
| Total Power per AFEE | 956 mW | |
| AFEE PCB, Qty 2 of 1.4 mil thick Copper Thermal Plane Layers. | | |

# AFEE FEMA Analysis

- **Failure Modes and Affects Analysis, Summary.** From LAT-TD-00464-03 2/03, Author Robert Prince, Swales Aerospace
- Per Cal unit, there are no single point failures
- Per Cal unit, several two point failure modes (single point per AFEE board)
- Single point failures per AFEE Board:
  - Power supply bypass capacitors
  - TEM command bus termination resistors
- TEM Components required for operational Cal unit not included in Cal FEMA calculations
  - TEM Power supply and fuses for Cal
  - Communication components for Cal
- Individual component failure rates, FITS values, determined from, or linkable to vendor data or MIL-HDBK-217F. ASICs, PIN Diode detectors and connectors FITs assumed

Cal FEMA Analysis Numbers

| Operational Mode | Calculated Reliability at end of 5 year operation |
|---|---|
| 15 / 16 functional units | > 0.98 (reqmt: > 0.96) |

# Electrical Procurement Status

- **Flight components being purchased**
  - Maxim MAX145 ADCs and MAX5121 DACs are on order
  - SLAC has ordered Novacap 56nF 250V capacitors
- **Flight Items remaining to purchase**
  - Printed circuit boards
  - Connectors
  - 50 Meg State of the Art resistors
  - Resistors
  - Capacitors
  - GCRC and GCFE Custom ASICs
  - 2.5V References

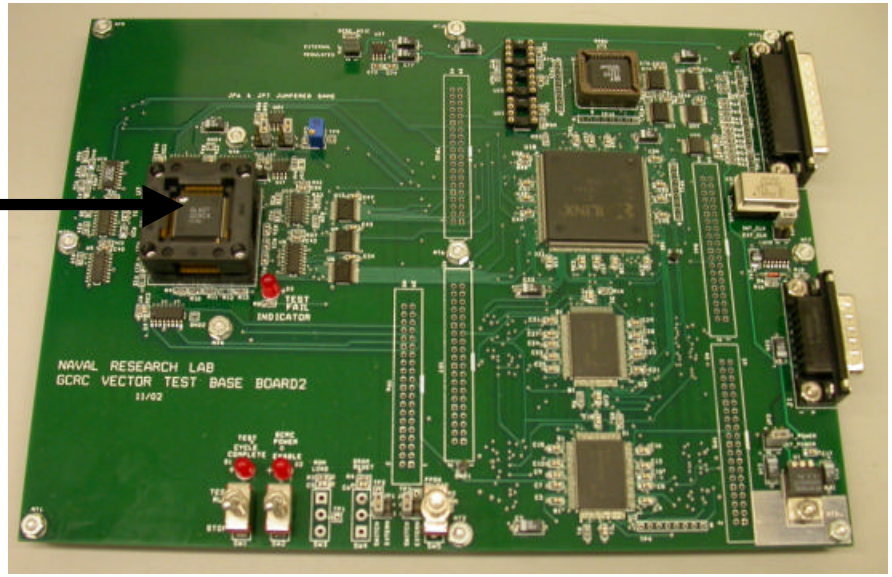
# Flight Component Screening, AFEE Board

- The AFEE Board Flight Assembly includes the flight AFEE – TEM cable
- Each Flight assembly will be mounted to a carrying frame, which supports both board and cable
- Each assembly will go through unpowered thermal cycles, 20 cycles, -30 to +85 degrees C
- Each assembly will go through powered dynamic burn in at 85 degrees C for 7 days
  - Test multiple assemblies simultaneously
  - Use extension cables with connector savers to TEMs outside of chamber
- Fabricate 100 AFEE Assemblies
  - Need 64 for Flight units, 8 for Qualification/Spare units
  - AFEE Assemblies failing testing are set aside
    - Won't be used without failure analysis, component replacement and requalification

# Flight Component Screening, GCRC ASIC

- Thermal cycle 100% GCRC ASICs unpowered, 20 cycles, –40 to +125 C
- 100% Functional Test Screening
  - NRL is completing development of high speed GCRC vector test board
    - Approximately 1000 parts
    - Test time per part less than 1 second
- 150 parts exposed to powered dynamic GCRC Burn in, 7 days, 100 degrees C
- Functional test of burn in parts following burn in testing
  - 52 of burned in chips sent for qualification testing
  - Remaining functional burned in chips become flight-ready spares

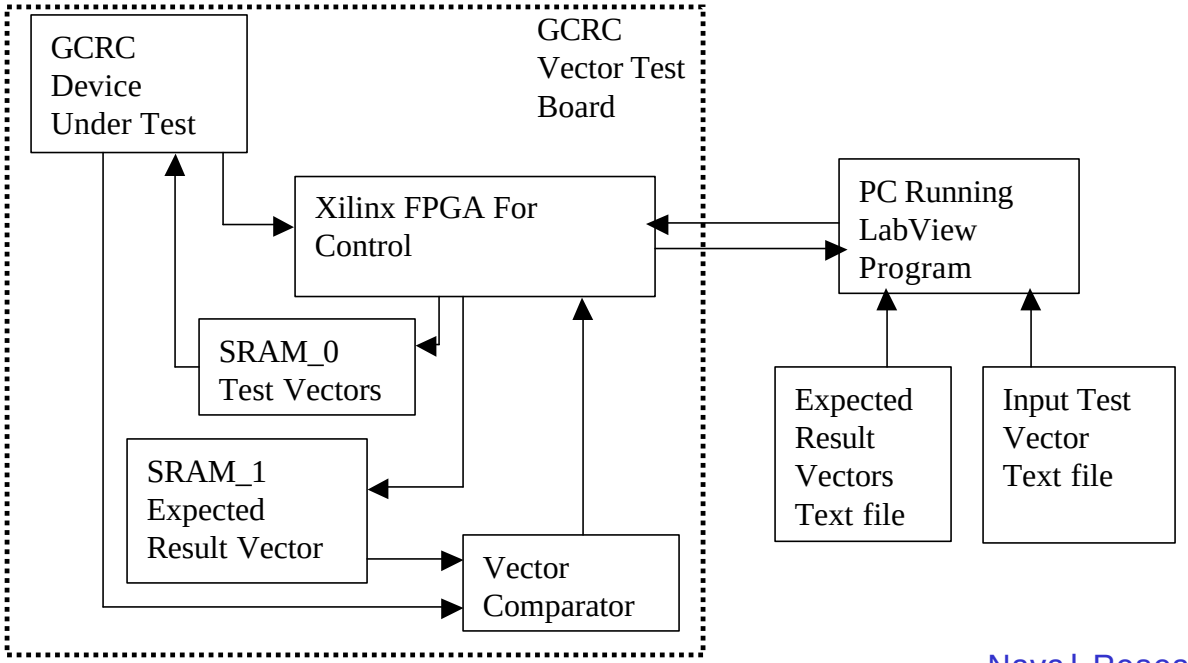
Chip Under Test




GCRC Vector Testboard 2

# GCRC Vector Testboard, Description

- Vector Test Board applies known test bits to GCRC ASIC input pins, every clock cycle
- Every clock cycle test board compares GCRC digital outputs to expected results vector
- Test vectors generated with VHDL testbench. Code Coverage tool used to ensure all GCRC VHDL code lines are tested
  - Need to improve testing to ensure that LVDS outputs come out quick enough for timing margins

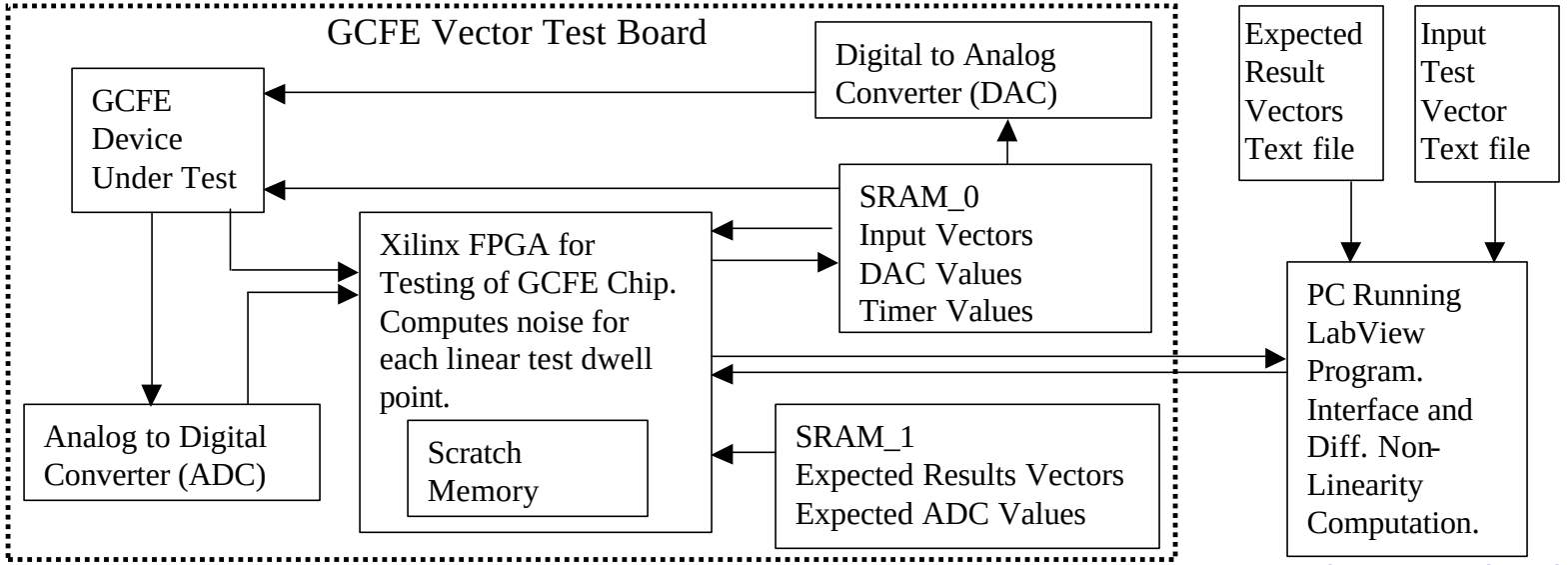


# Flight Component Screening, GCFE ASIC

- Thermal cycle 100% GCFE ASICs unpowered, 20 cycles, –40 to +125 C
- 100% Functional Test Screening
  - Approximately 6000 parts
  - NRL is developing high speed GCFE vector test board
- 10% powered dynamic GCFE Burn in, 7 days, 100 degrees C
- Functional test of burn in chips following burn in testing
  - 52 of burned in chips sent for qualification testing
  - Remaining functional burned in chips become flight-ready spares

# GCFE Vector Testboard, Description

- **Vector Testing for GCFE ASIC more difficult than GCRC testing**
  - **Testboard involves analog input and analog outputs**
  - **Do not have a VHDL analog model of the GCFE chip**
    - **Writing 'compiler' in 'C' that accepts high level commands and generates input test vectors and expected results vectors. Getting the compiler functioning correctly will be an iterative process**
  - **Initial GCFE ASIC testing has indicated that noise needs to be tested at every step of a linear sweep**
    - **Initial testboard design modified to be more comprehensive**
    - **Use local FPGA memory to store ADC values per linear sweep dwell point**
    - **FPGA calculates centroid and noise at each dwell point, send PC centroid value**
  - **First GCFE Vector Testboard Currently being assembled**



# Electrical Documentation Status

- **Major Documents Needed**
  - AFEE Components Radiation Test Plan
  - AFEE Board Part Radiation Susceptibility Analysis
  - AFEE Board Electrical Design Worst Case Analysis
  - AFEE Verification Plan
  - GCFE ASIC Verification Plan
  - GCFE ASIC Design Worst Case Analysis
  - GCRC ASIC Verification Plan
  - GCRC ASIC Design Worst Case Analysis

# Electrical Issues and Concerns, AFEE, ASICs

- **AFEE, GCRC and GCFE improvements for flight**
  - **GCRC, GCFE: LVDS communication**
    - **Have to test GCFEv9 and GCRCv5 chips for reliable communication with timing margin at 20 MHz. over temperature, voltage, and total dose**
    - **Expect problem to be solved with these new ASIC designs coming in from fabrication**
  - **GCFE, AFEE: calibration signal coupling**
    - **Signal picked up by non-strobed front-end chip is proportional to number of chips being strobed in the row, and amount of calibration charge injection**
      - **May be possible to severely attenuate coupling with additional on-board capacitors**
  - **GCFE: Output ringing**
    - **Have to test GCFEv9 analog output for elimination of oscillation problems**
      - **Expect problem to be solved with output buffer series resistance incorporated in GCFEv9**

# Electrical Issues and Concerns, Fusing

- **Fusing, current limiting**
  - **AFEE boards have no fusing and no device current limiting resistors**
  - **The TEM has individual fusing for each AFEE board**
  - **Reliability of CAL Modules for the Mission depends on the reliability of TEM fusing**